Datasheet

Creatcomm

CQM711 Bluetooth (BLE) Module

– Powered by Qualcomm QCC711

Table of Contents

1 Product Overview

Powered by Qualcomm QCC711, CQM711 modules are purposefully designed LGA form factor BLE modules that combine multi-core processing capabilities, high-security as well as BLE long-range to cater to the demands of diverse IoT applications. Their compact size and on-chip memory, including SRAM and RRAM (NVM), contribute to reducing costs and enhancing performance, making them an attractive choice for space-constrained IoT edge devices.

Unlike many other BLE modules on the market, CQM711 modules have integrated three processors – 64MHz Arm Cortex-M processor for application and 32MHz Arm Conrtex-M0 processor for BLE with shared on-chip memory of 128KB SRAM and 512KB RRAM. Additional Root-of-Trust 32MHz RISC-V processor with its own secure SRAM and ROM is dedicated to security subsystem to ensure the highest level of security for IoT applications with critical security needs. They have built-in resistive RAM (RRAM), the industry latest Non-volatile Memory (NVM) technology, eliminating need for externally attached NOR flash as well as resulting in more streamlined and cost-effective system. They also feature 3-wire and 4-wire SPI display control, making them capable of driving external LCD/TFT screens commonly found on a dedicated MCU. Furthermore, CQM711 modules can be powered directly by a battery, making it suitable for portable and battery-operated devices.

CQM711 can operate in hostless mode, capable of running both the Bluetooth stack and applications internally without requiring an external MCU. Moreover, they support hostless mode (HCI) through a UART interface, functioning as a Bluetooth transceiver to offload the Bluetooth stack. This enables the external MCU to focus on handling applications rather than managing the Bluetooth stack.

CQM711 modules include the following configurations:

Module	Form Factor	Antenna
CQM711-0-50-0P	12.19 x 12.19 x 2.2 mm, 1.27 mm pitch, 32-pin, LGA	Pin Antenna
CQM711-0-50-0B	12.19 x 16.24 x 2.2 mm, 1.27 mm pitch, 32-pin, LGA	PCB Antenna
CQM711-0-50-0U	12.19 x 16.24 x 2.2 mm, 1.27 mm pitch, 32-pin, LGA	U.FL Antenna

CQM711 module portfolio is graphically illustrated below:

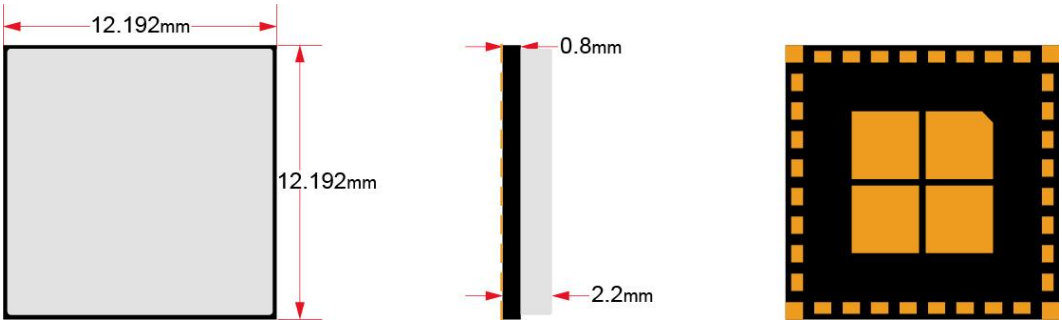

Figure 1: CQM711-0-50-0P Module View

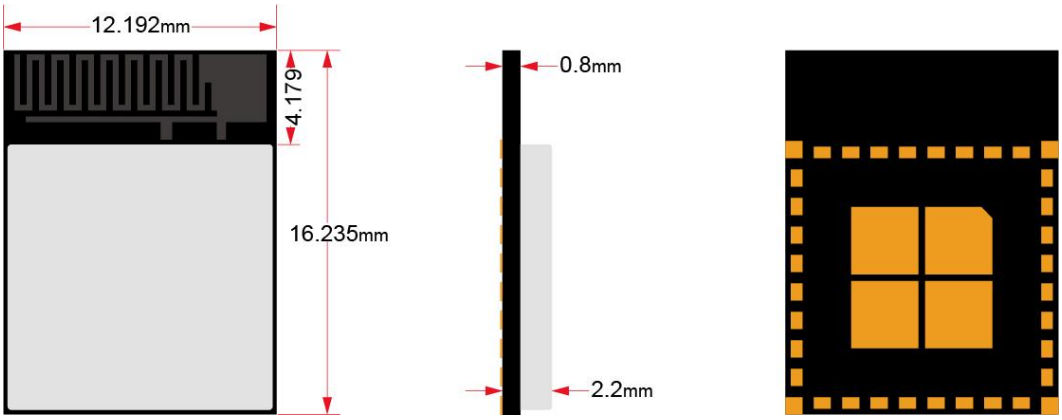

Figure 2: CQM711-0-50-0B Module View

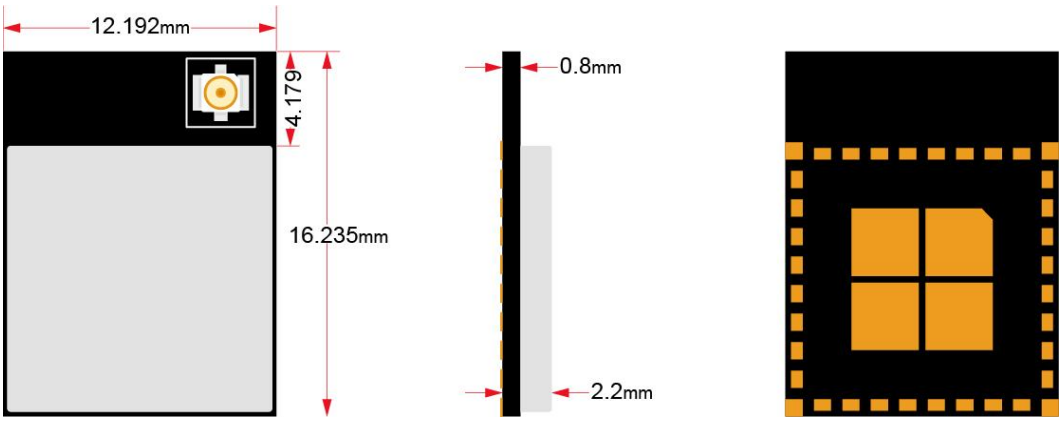

Figure 3: CQM711-0-50-0U Module View

The module specific development kit is also provided to facilitate application software development as shown below:

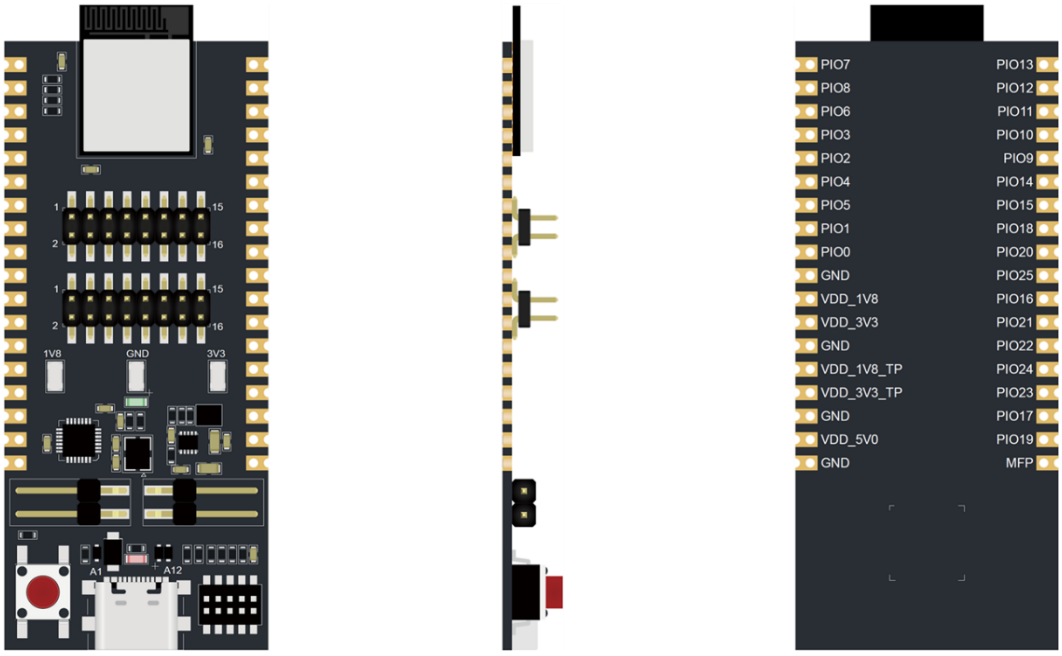

Figure 4: CQM711 Module Development Kit

2 Hardware Specification

This section provides detailed hardware design and specification of CQM711 modules. CQM711 hardware design has been optimized for small footprint and reduced RBOM cost.

2.1 Block Diagram

CQM711 integrates 4MB NOR flash and a 32.768kHz RTC crystal as optional components. The design also supports PCB antenna (CQM711-0-50-0B) or simply provides antenna pin (CQM711-0-50-0U) to allow customized antenna implementation on motherboard. The block diagram is shown below.

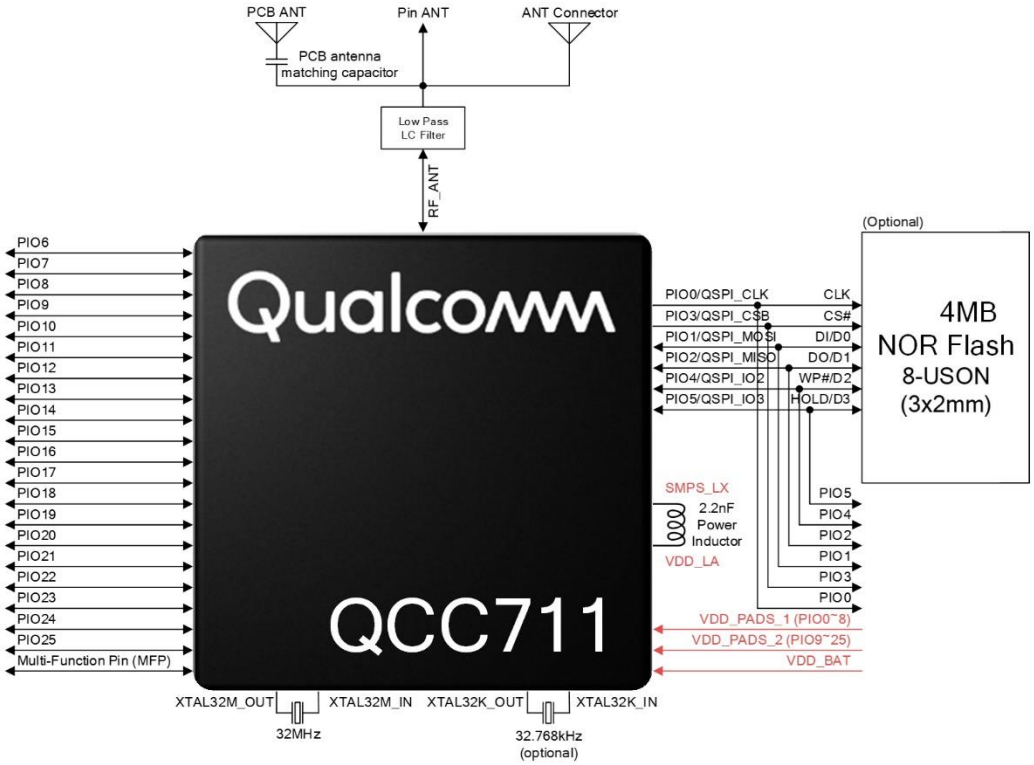

Figure 5: CQM711 Module Block Diagram

2.2 Pinout Description

2.2.1 Pin Map

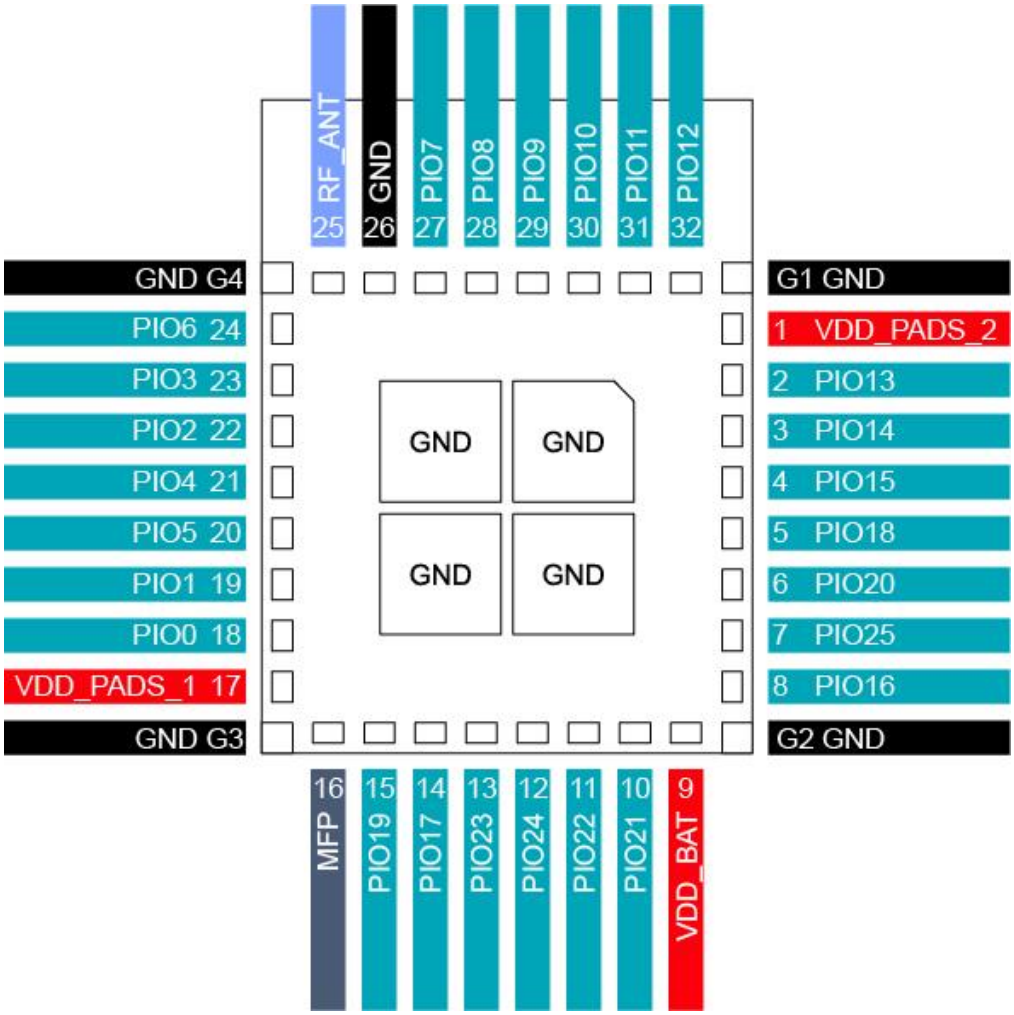

Figure 6: CQM711-0-50-0P Module Pin Map

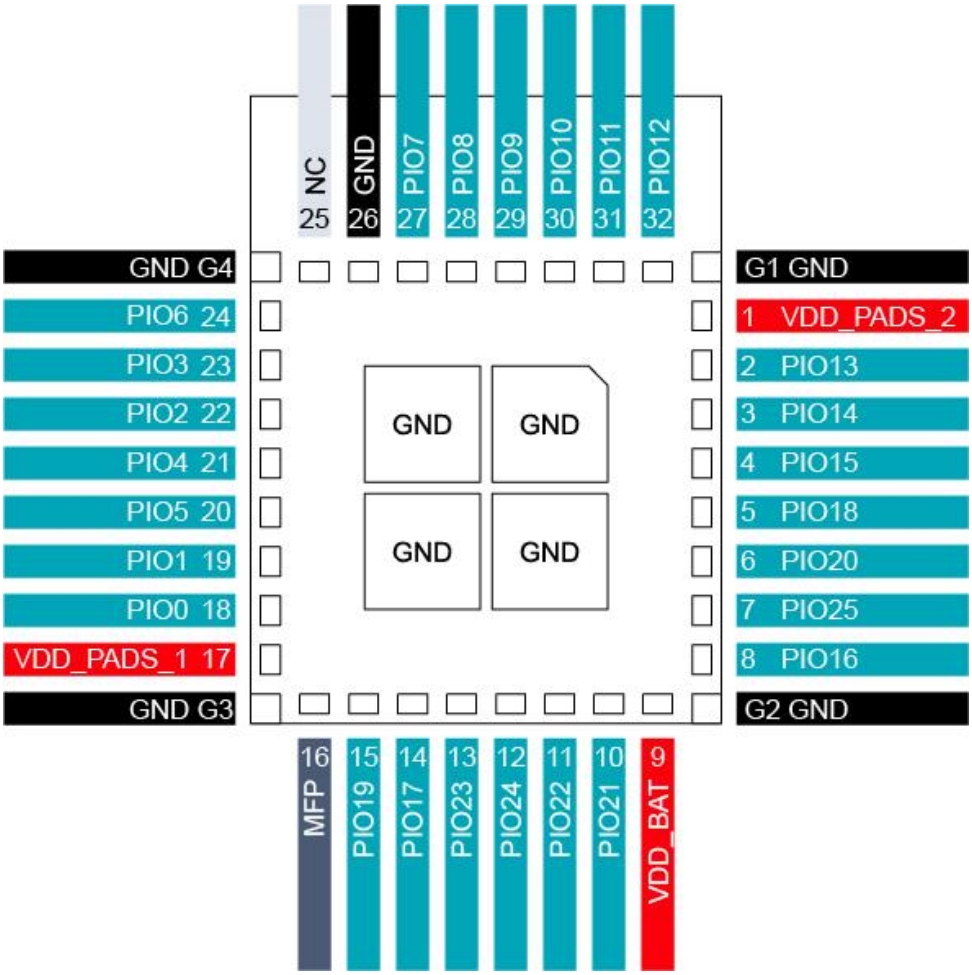

Figure 7: CQM711-0-50-0B/U Module Pin Map

2.2.2 Pin Definition

Pin	Pin Name	Type	Power Domain	Description
9	VDD_VBAT	PWR	-	Power input (1.71~3.6V)
17	VDD_PADS_1	PWR	-	Host I/O voltage input (≤ VDD_VBAT)
1	VDD_PADS_2	PWR	-	Host I/O voltage input (≤ VDD_VBAT)
G1-G4,26	GND	GND	GND	Ground
25	RF_ANT	AI/AO	-	Pin antenna(CQM711-0-50-0P)
	NC	-	-	No Connection(CQM711-0-50-0B/U)
16	MFP	DI	VDD_VBATT	SW configurable as a reset input
18	PIO0	DI/DO	VDD_PADS_1	Generic PIO
19	PIO1	DI/DO	VDD_PADS_1	Generic PIO
22	PIO2	DI/DO	VDD_PADS_1	Generic PIO

23	PIO3	DI/DO	VDD_PADS_1	Generic PIO
21	PIO4	DI/DO	VDD_PADS_1	Generic PIO
20	PIO5	DI/DO	VDD_PADS_1	Generic PIO
24	PIO6	DI/DO	VDD_PADS_1	Generic PIO
27	PIO7	DI/DO	VDD_PADS_1	Generic PIO
28	PIO8	DI/DO	VDD_PADS_1	Generic PIO
29	PIO9	DI/DO	VDD_PADS_2	Generic PIO
30	PIO10	DI/DO	VDD_PADS_2	Generic PIO
31	PIO11	DI/DO	VDD_PADS_2	Generic PIO
32	PIO12	DI/DO	VDD_PADS_2	Generic PIO
2	PIO13	DI/DO	VDD_PADS_2	Generic PIO
3	PIO14	DI/DO	VDD_PADS_2	Generic PIO
4	PIO15	DI/DO	VDD_PADS_2	Generic PIO
8	PIO16	DI/DO	VDD_PADS_2	Generic PIO
14	PIO17	DI/DO	VDD_PADS_2	Generic PIO
5	PIO18	DI/DO	VDD_PADS_2	Generic PIO
15	PIO19	DI/DO	VDD_PADS_2	Generic PIO
6	PIO20	DI/DO	VDD_PADS_2	Generic PIO
10	PIO21	DI/DO	VDD_PADS_2	Generic PIO
11	PIO22	DI/DO	VDD_PADS_2	Generic PIO, analog in configurable
13	PIO23	DI/DO	VDD_PADS_2	Generic PIO, analog in configurable
12	PIO24	DI/DO	VDD_PADS_2	Generic PIO, analog in configurable
7	PIO25	DI/DO	VDD_PADS_2	Generic PIO, analog in configurable

2.2.3 I/O Pin Mux Table

GPIO	QSPI	I2C	FTC	LED	Analog	CoEx	Debug	SE0	SE1	SE2	SE3
PIO0	QSPI_CLK	SDA	ftc0_out	BLUE				Port 0	Port 0	Port 0	Port 0
PIO1	QSPI_MOSI	SCL	ftc0_out	RED				Port 1	Port 1	Port 1	Port 1
PIO2	QSPI_MISO	SDA	ftc0_out	GREEN				Port 2	Port 2	Port 2	Port 2
PIO3	QSPI_CSB	SCL	ftc1_out	WHITE				Port 3	Port 3	Port 3	Port 3
PIO4	QSPI_IO2	SDA	ftc1_out	WHITE				Port 0	Port 4	Port 4	Port 4
PIO5	QSPI_IO3	SCL	ftc1_out	BLUE				Port 1	Port 0	Port 0	Port 0
PIO6		SDA	ftc_in	RED				Port 2	Port 1	Port 1	Port 1
PIO7		SCL		GREEN				Port 3	Port 2	Port 2	Port 2

PIO8								Port 4	Port 3	Port 3	Port 3
PIO9							TCK/SWD_CLK		Port 4	Port 4	Port 4
PIO10							TMS/SWD_DIO		Port 0	Port 0	Port 0
PIO11	QSPI_CLK	SDA	ftc_in				TDI/test_hf	Port 0	Port 1	Port 1	Port 1
PIO12	QSPI_MOSI	SCL					TDO/SWO	Port 1	Port 2	Port 2	Port 2
PIO13	QSPI_MISO	SDA	ftc2_out				Test_lf	Port 2	Port 3	Port 3	Port 3
PIO14	QSPI_CSB	SCL	ftc2_out					Port 3	Port 4	Port 4	Port 4
PIO15	QSPI_IO2	SDA	ftc2_out	BLUE/WHITE			trace_ctrl	Port 4		Port 3	Port 3
PIO16	QSPI_IO3	SCL	ftc_in	RED/WHITE			trace_clk	Port 0	Port 0	Port 1	Port 1
PIO17		SDA	ftc3_out	GREEN/WHITE			trace_data_0	Port 1	Port 1	Port 2	Port 2
PIO18		SCL	ftc3_out	WHITE			trace_data_1	Port 2	Port 2	Port 3	Port 3
PIO19		SDA	ftc3_out	WHITE			trace_data_2	Port 3	Port 3	Port 4	Port 4
PIO20		SCL		WHITE		slv_pta_coex_active	trace_data_3	Port 4	Port 4		
PIO21		SDA	ftc_in	WHITE		slv_pta_coex_status		Port 0	Port 0	Port 0	Port 0
PIO22		SCL		BLUE	ADC	slv_pta_coex_confx		Port 1	Port 1	Port 1	Port 1
PIO23		SDA		RED	ADC	mstr_pta_coex_active		Port 2	Port 2	Port 2	Port 2
PIO24		SCL		GREEN	ADC	mstr_pta_coex_status		Port 3	Port 3	Port 3	Port 3
PIO25				WHITE	ADC	mstr_pta_coex_confx		Port 4	Port 4	Port 4	Port 4

2.2.4 Programmable Series Engine

Serial Engines (SE) and supported interfaces

SE	3-wire or 4-wire SPI Display Controller	True 4-wire SPI Controller/Peripheral	I2C Controller	8-bit UART	9-bit UART
SE0	Yes	Yes	Yes	Yes	Yes
SE1	Yes	Yes	Yes	Yes	Yes
SE2	-	-	Yes	Yes	-
SE3	-	-	Yes	Yes	-

Serial engines default port mappings

SE	3-wire Display	4-wire Display	I2C	UART	SE0 true 4-wire SPI
Port 0	CS1	CS1	SDA	CTS	MISO
Port 1	SDIN	SDIN	SCL	RTS	MOSI
Port 2	CLK	CLS	-	TXD	CLS

Port 3	CS	CS	-	RXD	CS
Port 4		D/C	-	-	CS1

2.3 Computing Subsystem

2.3.1 Microcontroller

CQM711 modules have Qualcomm QCC711 at his core which integrates three microcontrollers – Arm Cortex-M3 processor, Arm Cortex-M0 processor, and RISC-V:

Arm Cortex-M3 processor – Running at 32MHz, dedicated to higher layer protocol and user applications. It conducts inter-processor communication with Arm Cortec-M0 processor for BLE services and with RISC-V processor for security services.

Arm Cortex-M0 processor – Running at 32MHz, dedicated to BLE radio and lower protocol layer (MAC) processing.

RISC-V processor – Running at 32MHz, dedicated to security services. it can function as a Root-of-Trust (RoT) processor to execute highly secure bootup code under Trusted Execution Environment (TEE) that validate the user application image before handing over the control to Arm Cortex-M3 processor. RISC-V has its own 32KB SRAM, 192KB ROM and protected OTP area and will be NOT visible to user applications, making it highly reliable and secure.

The computing subsystem software architecture consists of three parts as illustrated below. Computing Subsystem (APSS) has been open-sourced on GitHub while Bluetooth Subsystem (BTSS) and Security Subsystem will be offered in binary format inside software SDK package.

GitHub Download Link: *https://github.com/quic/qccsdk-qcc711/*

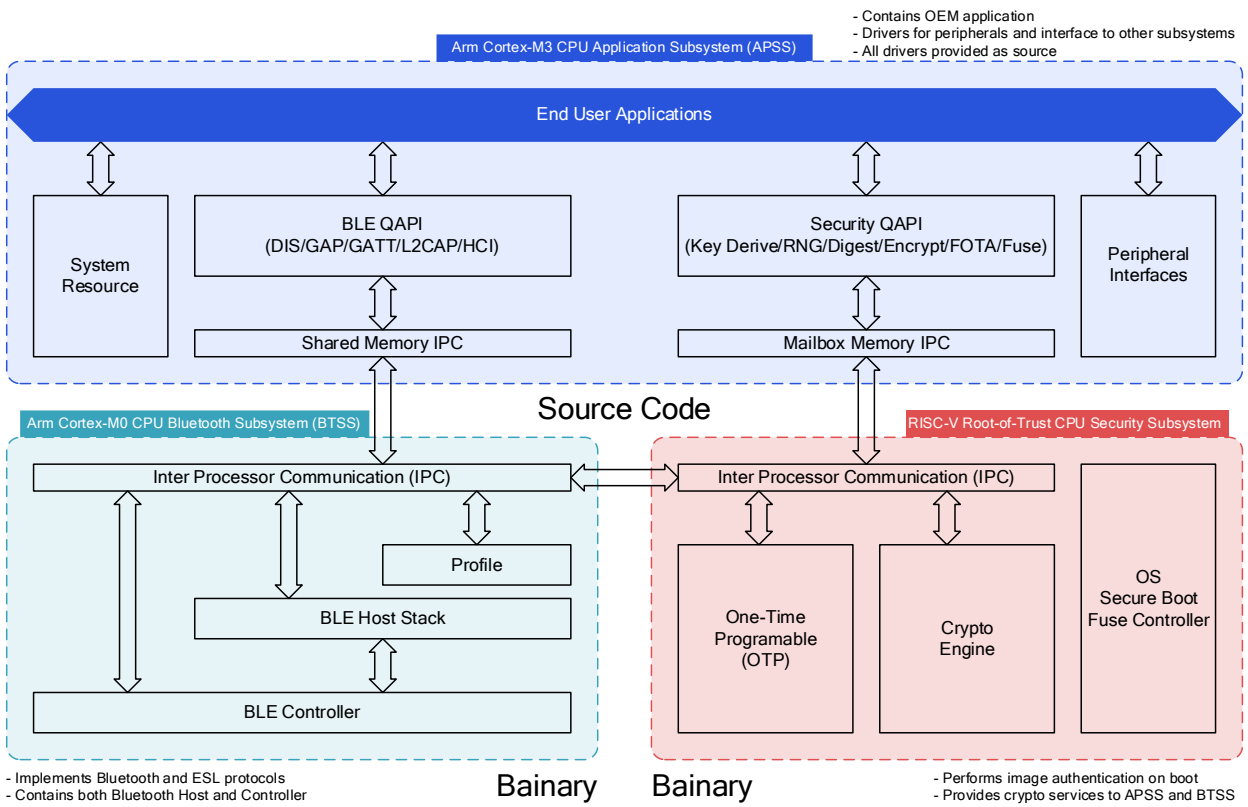

Figure 8: Computing Subsystem Software Architecture

2.4 Memory

There are 512KB on-chip RRAM, 128KB on-chip SRAM and 2KB OTP/MTP shared among three processors. Built-in Non-volatile memory RRAM hosting execution code will eliminate needs of an external NOR flash to reduce system cost.

Additional NOR flash can be added through QSPI interface for additional data storage.

2.5 Peripheral Interfaces

CQM711 modules supports the following peripheral interfaces through 26x configurable PIO:

- 2x SPI master or slave, support 3-wire/4-wire SPI for display and true 4-wire SPI with DMA
- 2x I2C master and 1x I2C slave, supporting 100kbps, 400kbps, and 1000kbps data rate
- 2x 9-bit UART with hardware flow control, supporting maximum 2M baud rate

- 1x 8-bit UART with hardware flow control, supporting maximum 2M baud rate
- 4x 10-bit ADC
- 4x FTC (PWM)
- 4x LED driver
- 3-wire PTA coexistence master or slave
- SWD with 4-bit trace

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

The absolute maximum ratings provided in this section reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating specifications.

Pin	Parameter	Min	Max	Unit
VDD_VBATT	Power input voltage	VDD_PADS_2	3.63	V
VDD_PADS_1	I/O port 1 voltage	VSS - 0.3	3.63	V
VDD_PADS_2	I/O port 2 voltage	VSS - 0.3	3.63	V
Digital I/O	PIO25:PIO9	VSS - 0.3	VDD_PADS_2 + 0.3	V
	PIO8:PIO0	VSS - 0.3	VDD_PADS_1 + 0.3	V
	MFP	VSS - 0.3	VDD_VBAT + 0.3	V
All ground / VSS pads	-	0	0	V
Storage temperature	-	-40	85	°C

3.2 Recommended Operating Conditions

Pin	Parameter	Min	Max	Unit
VDD_VBATT	Power input voltage	1.71	3.6	V
VDD_PADS_1	I/O port 1 voltage	0	3.6	V
VDD_PADS_2	I/O port 2 voltage	0	3.6	V
Digital I/O	PIO25:PIO9	VSS	VDD_PADS_2	V
	PIO8:PIO0	VSS	VDD_PADS_1	V
	MFP	VSS	VDD_VBAT	V

All ground / VSS pads	-	0	0	V
Operating temperature	-	-40	85	°C
Storage temperature	-	-40	85	°C

4 Radio Performance

Channel Bandwidth	Modulation	Parameter	Data Rate	Typical	Unit
2MHz	GFSK	Tx Power	2Mbps	+6.5	dBm
			1Mbps	+6.5	dBm
			500kbps	+6.5	dBm
			125kbps	+6.5	dBm
		Rx Sensitivity @ 30.8% PER (Boost Mode)	2Mbps	-93.5	dBm
			1Mbps	-98.0	dBm
			500kbps	-100.5	dBm
			125kbps	-107.5	dBm
		Rx Sensitivity @ 30.8% PER (Normal Mode)	2Mbps	-90.0	dBm
			1Mbps	-95.0	dBm
			500kbps	-97.5	dBm
			125kbps	-104.0	dBm
Note: Measured using test packets with 37 octet payload, VBATT = 3.0V					

5 Power Consumption

CQM711 modules can operate in four power states as shown below to maximize power saving:

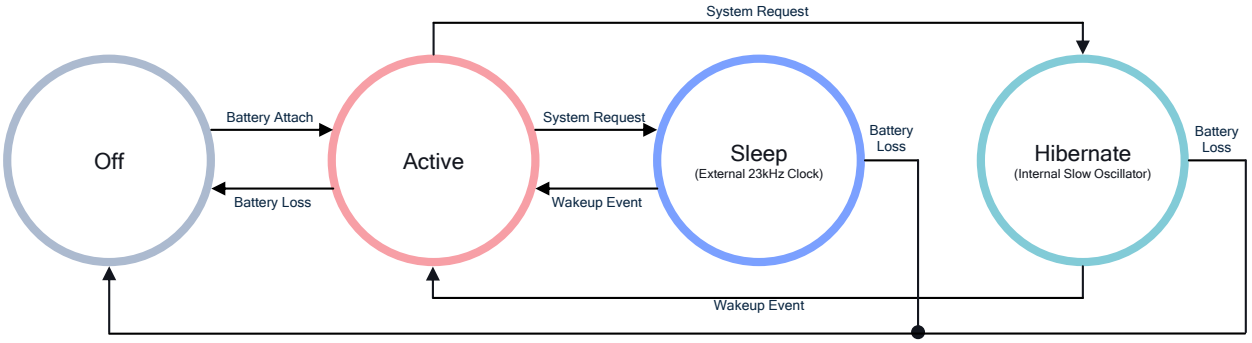

Figure 9: Power State Diagram

5.1 Active Power

Channel Bandwidth	Modulation	Parameter	dBm	Average Current	Unit
2MHz	GFSK	Tx Power	0	10.5	mA
			+4	14.6	mA
			+6	16.6	mA
		Rx Power Normal	TBD	TBD	mA
		Rx Power Boost	-95	5.3	mA

5.2 Sleep Power

Test Mode	MCU State	Average Current	Unit
• Software controlled • 16KB SRAM retained • 32kHz crystal running • Measured from the SDK - once connected to an AP	Sleep	4	µA
• Software controlled • No SRAM retained	Hibernate	16	µA

• Internal LFLPO running • Measured from the SDK - not connected to an AP			

6 Mechanical Specification

6.1 Pin Antenna

6.1.1 Dimension

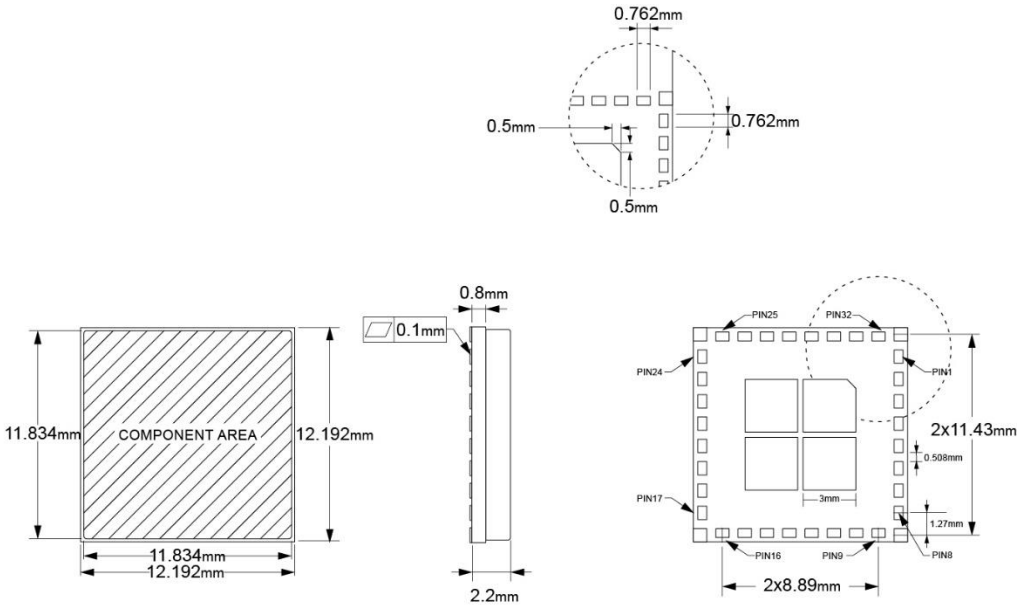

Figure 10: CQM711-0-50-0P Module Dimension

6.1.2 Recommended PCB Landing Pattern

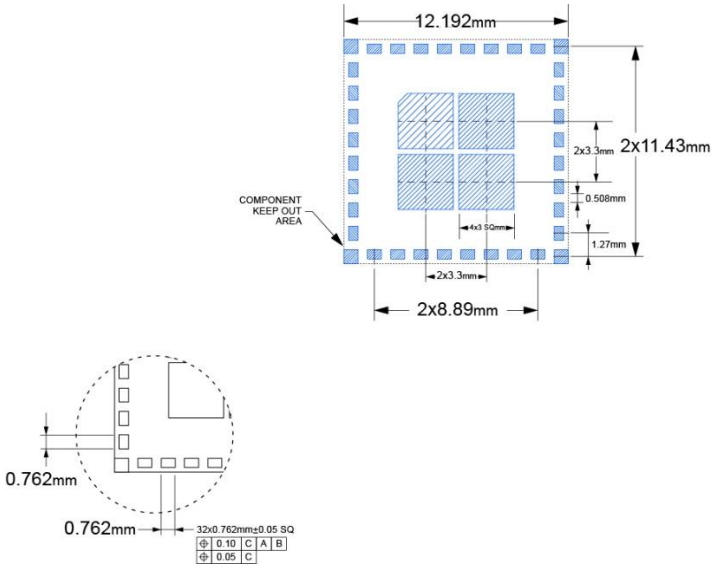

Figure 11: CQM711-0-50-0P Module PCB Landing Pattern

6.2 PCB Antenna

6.2.1 Dimension

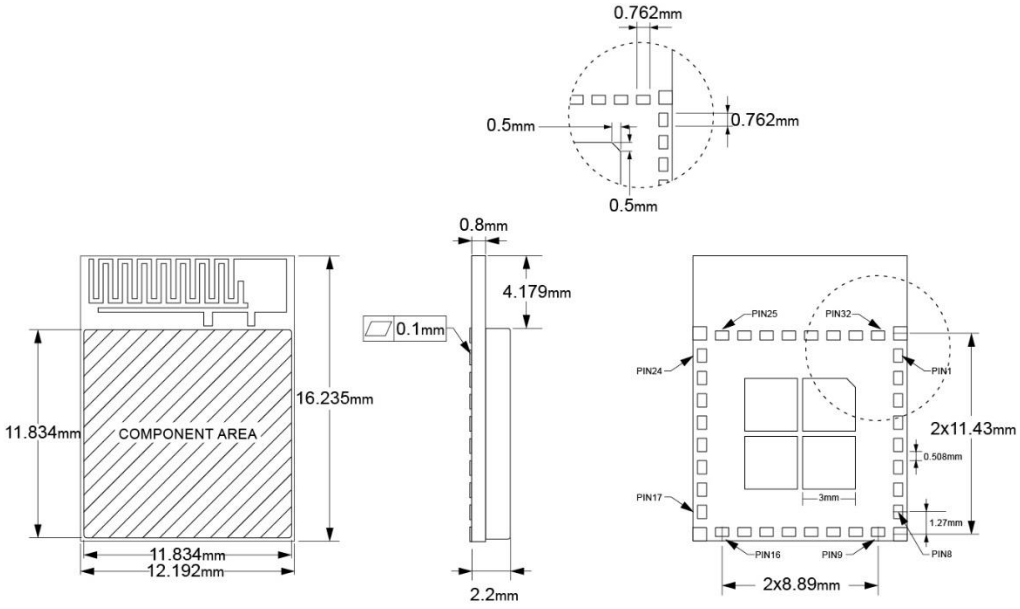

Figure 12: CQM711-0-50-0B Module Dimension

6.2.2 Recommended PCB Landing Pattern

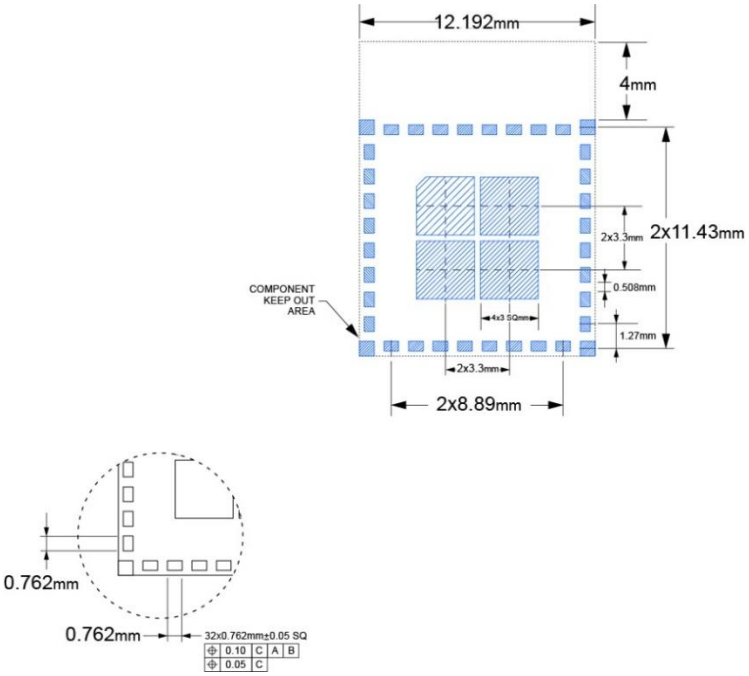

Figure 13: CQM711-0-50-0B Module PCB Landing Pattern

6.3 Connector Antenna

6.3.1 Dimension

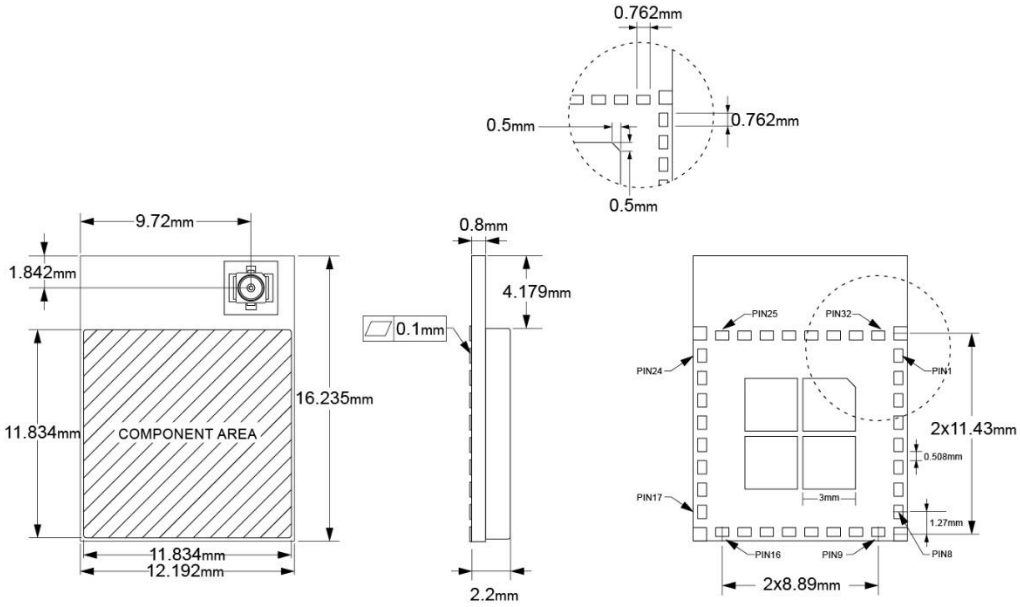

Figure 14: CQM711-0-50-0U Module Dimension

6.3.2 Recommended PCB Landing Pattern

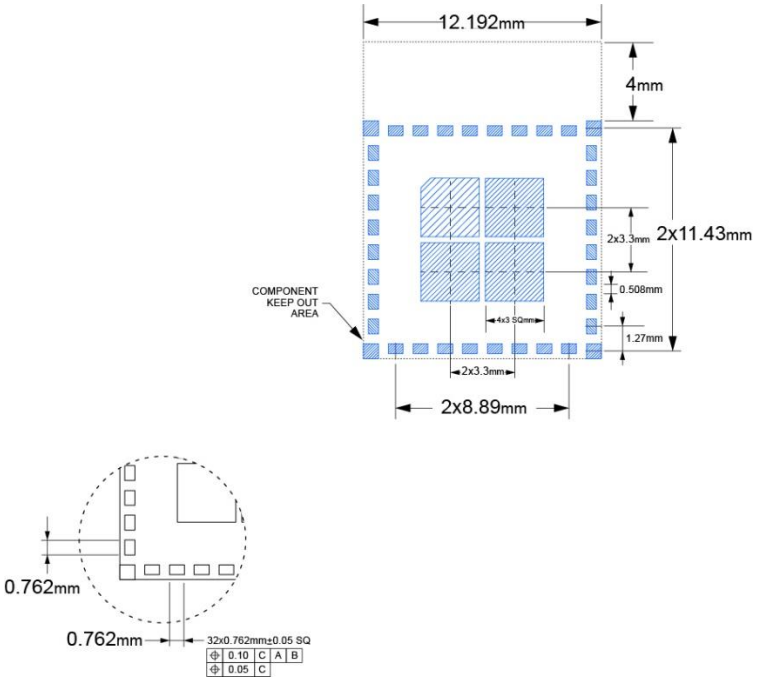

Figure 15: CQM711-0-50-0U Module PCB Landing Pattern

7 Manufacturing Recommendation

7.1 Power Layout Guideline

CQM711 modules are powered by either 3V battery or DC 3.3V. Power pin connection capacitor is as close as possible to chip and pin. Decoupling the power supply from the chip using a capacitor. Use capacitors to prevent noise from coupling back to the power plane.

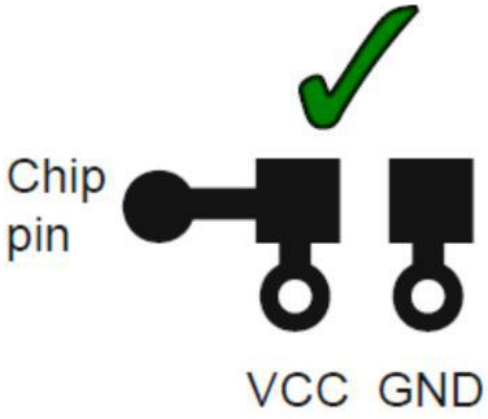

Figure 16: Power Layout Guideline

7.2 Soldering Recommendations

CQM711 modules can be SMT on the board following the temperature curve graph:

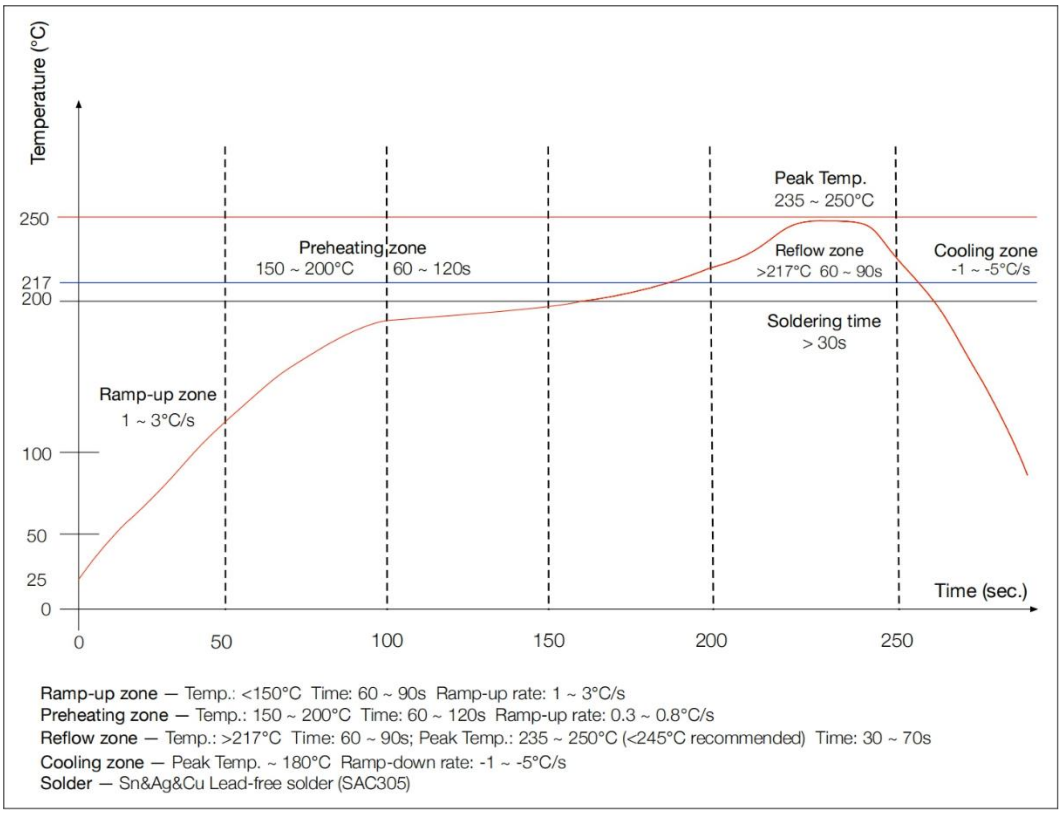

Figure 17: Soldering Guideline

Revision History

Revision	Description	Date
1.0	Initial draft	July 1, 2024
1.1	Update size and pin map	Jan 14, 2025
1.2	Update Module name	Mar 18, 2025

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